



FEATURES

- Input overvoltage protection, 32 V above and below the supply rails
- No phase reversal for input voltage up to ± 32 V beyond the power supply
- Rail-to-rail input and output swing
- Low power: 60 μ A per amplifier typical
- Unity-gain bandwidth
- 800 kHz typical at $V_{SY} = \pm 15$ V
- 550 kHz typical at $V_{SY} = \pm 5$ V
- 465 kHz typical at $V_{SY} = \pm 1.5$ V
- Single-supply operation: 3 V to 30 V
- Low offset voltage: 300 μ V maximum
- Large signal voltage gain: 120 dB typical
- Unity gain stable
- Qualified for automotive applications

APPLICATIONS

- Battery monitoring
- Sensor conditioners
- Portable power supply controls
- Portable instrumentation

GENERAL DESCRIPTION

The ADA4096-2 dual and ADA4096-4 quad operational amplifiers feature micropower operation and rail-to-rail input and output ranges. The extremely low power requirements and guaranteed operation from 3 V to 30 V make these amplifiers perfectly suited to monitor battery usage and to control battery charging. Their dynamic performance, including 27 nV/ $\sqrt{\text{Hz}}$ voltage noise density, recommends them for battery-powered audio applications. Capacitive loads to 200 pF are handled without oscillation.

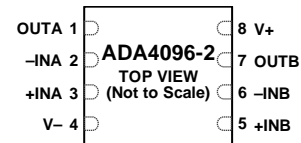
The ADA4096-2 and ADA4096-4 have overvoltage protection inputs and diodes that allow the voltage input to extend 32 V above and below the supply rails, making this device ideal for robust industrial applications. The ADA4096-2 and ADA4096-4 feature a unique input stage that allows the input voltage to exceed either supply safely without any phase reversal or latch-up; this is called overvoltage protection, or OVP.

The dual ADA4096-2 is available in 8-lead LFCSP (2 mm \times 2 mm) and 8-lead MSOP packages. The ADA4096-2 is available in 16-lead LFCSP (3 mm \times 3 mm) and 14-lead TSSOP packages. The ADA4096-2W is qualified for automotive applications and is available in an 8-lead MSOP package.

PIN CONNECTION DIAGRAMS



Figure 1. 8-Lead, MSOP (RM-8), ADA4096-2



NOTES
1. CONNECT THE EXPOSED PAD TO V-.

Figure 2. 8-Lead LFCSP (CP-8-10), ADA4096-2

Note: For the ADA4096-4, see the Pin Configurations and Function Descriptions section.

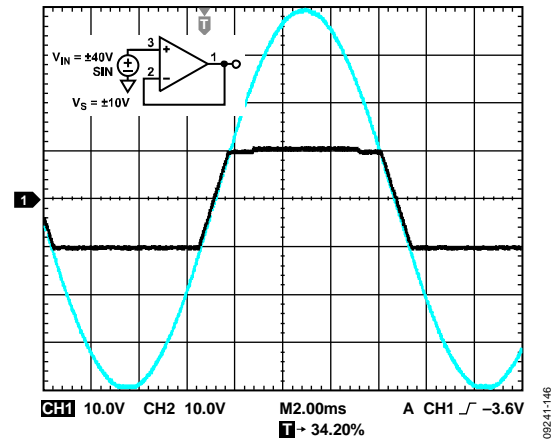


Figure 3. No Phase Reversal

The ADA409x family is specified over the extended industrial temperature range of $(-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$) and is part of the growing selection of 30 V, low power op amps from Analog Devices, Inc. (see Table 1).

Table 1. Low Power, 30 V Operational Amplifiers

| Op Amp | Rail-to-Rail I/O | PJFET | Low Noise |
|--------|------------------|--------|-----------|
| Dual | ADA4091-2 | AD8682 | AD8622 |
| Quad | ADA4091-4 | AD8684 | AD8624 |

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REVISION HISTORY

12/14—Rev. E to Rev. F

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3/14—Rev. D to Rev. E

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5/13—Rev. C to Rev. D

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8/12—Rev. A to Rev. B

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3/12—Rev. 0 to Rev. A

Changed -3 dB Closed-Loop Bandwidth from 97 kHz to
 970 kHz, Table 2.....3
 Changed -3 dB Closed-Loop Bandwidth from 114 kHz to
 1140 kHz, Table 34
 Changed to -3 dB Closed-Loop Bandwidth from 152 kHz to
 1520 kHz, Table 45
 Updated Outline Dimensions 18

7/11—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS, $V_{SY} = \pm 1.5\text{ V}$

$V_{SY} = \pm 1.5\text{ V}$, $V_{CM} = V_{SY}/2$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 2.

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|------------------------------|--------------------------|--|------|-----------|-----------|------------------------------|
| INPUT CHARACTERISTICS | | | | | | |
| Offset Voltage | V_{OS} | $0^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | | 35 | 300 | μV |
| | | $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | | | 450 | μV |
| Offset Voltage Drift | $\Delta V_{OS}/\Delta T$ | $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | | 1 | 900 | $\mu\text{V}/^\circ\text{C}$ |
| Input Bias Current | I_B | $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | | ± 10 | ± 25 | nA |
| | | | | | ± 30 | nA |
| Input Offset Current | I_{OS} | $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | | ± 0.1 | ± 1.5 | nA |
| | | | | | ± 3 | nA |
| Input Voltage Range | | | -1.5 | | +1.5 | V |
| Common-Mode Rejection Ratio | CMRR | $V_{CM} = 0\text{ V to } \pm 1.5\text{ V}$ | 61 | 77 | | dB |
| | | $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | 58 | | | dB |
| Large Signal Voltage Gain | A_{VO} | $R_L = 10\text{ k}\Omega$, $V_O = -1.4\text{ V to } +1.4\text{ V}$ | 91 | 94 | | dB |
| | | $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | 84 | | | dB |
| | | $R_L = 2\text{ k}\Omega$, $V_O = -1.3\text{ V to } +1.3\text{ V}$ | 86 | 92 | | dB |
| | | $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | 77 | | | dB |
| MATCHING CHARACTERISTICS | | | | | | |
| Offset Voltage | | $T_A = 25^\circ\text{C}$ | | 100 | 300 | μV |
| OUTPUT CHARACTERISTICS | | | | | | |
| Output Voltage High | V_{OH} | $R_L = 10\text{ k}\Omega$ to GND | 1.48 | 1.49 | | V |
| | | $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | 1.45 | | | V |
| | | $R_L = 2\text{ k}\Omega$ to GND | 1.45 | 1.46 | | V |
| | | $-40^\circ\text{C to } +125^\circ\text{C}$ | 1.40 | | | V |
| Output Voltage Low | V_{OL} | $R_L = 10\text{ k}\Omega$ to GND | | -1.49 | -1.48 | V |
| | | $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | | | -1.45 | V |
| | | $R_L = 2\text{ k}\Omega$ to GND | | -1.48 | -1.47 | V |
| | | $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | | | -1.40 | V |
| Short-Circuit Limit | I_{SC} | Source/sink | | ± 10 | | mA |
| Closed-Loop Impedance | Z_{OUT} | $f = 100\text{ kHz}$, $A_V = 1$ | | 102 | | Ω |
| POWER SUPPLY | | | | | | |
| Power Supply Rejection Ratio | PSRR | $V_{SY} = 3\text{ V to } 36\text{ V}$ | 100 | | | dB |
| | | $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | 90 | | | dB |
| Supply Current per Amplifier | I_{SY} | $V_O = V_{SY}/2$ | | 40 | 50 | μA |
| | | $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | | | 80 | μA |
| DYNAMIC PERFORMANCE | | | | | | |
| Slew Rate | SR | $R_L = 100\text{ k}\Omega$, $C_L = 30\text{ pF}$ | | 0.25 | | V/ μs |
| Gain Bandwidth Product | GBP | $V_{IN} = 5\text{ mV p-p}$, $R_L = 10\text{ k}\Omega$, $A_V = 100$ | | 501 | | kHz |
| Unity-Gain Crossover | UGC | $V_{IN} = 5\text{ mV p-p}$, $R_L = 10\text{ k}\Omega$, $A_V = 1$ | | 465 | | kHz |
| Phase Margin | Φ_M | | | 51 | | Degrees |
| -3 dB Closed-Loop Bandwidth | $f_{-3\text{ dB}}$ | $A_V = 1$, $V_{IN} = 5\text{ mV p-p}$ | | 970 | | kHz |
| NOISE PERFORMANCE | | | | | | |
| Voltage Noise | e_n p-p | 0.1 Hz to 10 Hz | | 0.7 | | $\mu\text{V p-p}$ |
| Voltage Noise Density | e_n | $f = 1\text{ kHz}$ | | 27 | | nV/ $\sqrt{\text{Hz}}$ |
| Current Noise Density | i_n | $f = 1\text{ kHz}$ | | 0.2 | | pA/ $\sqrt{\text{Hz}}$ |

ELECTRICAL SPECIFICATIONS, $V_{SY} = \pm 5\text{ V}$

$V_{SY} = \pm 5\text{ V}$, $V_{CM} = V_{SY}/2$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 3.

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---------------------------------|--------------------------|--|------|-----------|----------|------------------------------|
| INPUT CHARACTERISTICS | | | | | | |
| Offset Voltage | V_{OS} | $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | | 35 | 300 | μV |
| Offset Voltage Drift | $\Delta V_{OS}/\Delta T$ | | | 1 | 500 | $\mu\text{V}/^\circ\text{C}$ |
| Input Bias Current | I_B | $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | | ± 10 | ± 25 | nA |
| Input Offset Current | I_{OS} | $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | | ± 1.5 | ± 2 | nA |
| Input Voltage Range | | | -5 | | +5 | V |
| Common-Mode Rejection Ratio | CMRR | $V_{CM} = -5\text{ V to }+5\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | 72 | 86 | | dB |
| | | $V_{CM} = -3\text{ V to }+3\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | 68 | 103 | | dB |
| | | $V_{CM} = -3\text{ V to }+3\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | 91 | 103 | | dB |
| | | $V_{CM} = -3\text{ V to }+3\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | 85 | | | dB |
| Large Signal Voltage Gain | A_{VO} | $R_L = 10\text{ k}\Omega$, $V_O = \pm 4.8\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | 102 | 111 | | dB |
| | | $R_L = 2\text{ k}\Omega$, $V_O = \pm 4.7\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | 99 | | | dB |
| | | $R_L = 2\text{ k}\Omega$, $V_O = \pm 4.7\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | 93 | 103 | | dB |
| | | $R_L = 2\text{ k}\Omega$, $V_O = \pm 4.7\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | 88 | | | dB |
| MATCHING CHARACTERISTICS | | | | | | |
| Offset Voltage | | $T_A = 25^\circ\text{C}$ | | 100 | 300 | μV |
| OUTPUT CHARACTERISTICS | | | | | | |
| Output Voltage High | V_{OH} | $R_L = 10\text{ k}\Omega$ to GND $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | 4.96 | 4.97 | | V |
| | | $R_L = 2\text{ k}\Omega$ to GND $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | 4.95 | | | V |
| | | $R_L = 2\text{ k}\Omega$ to GND $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | 4.80 | 4.90 | | V |
| | | $R_L = 2\text{ k}\Omega$ to GND $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | 4.70 | | | V |
| Output Voltage Low | V_{OL} | $R_L = 10\text{ k}\Omega$ to GND $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | | -4.98 | -4.97 | V |
| | | $R_L = 10\text{ k}\Omega$ to GND $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | | | -4.95 | V |
| | | $R_L = 2\text{ k}\Omega$ to GND $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | | -4.90 | -4.80 | V |
| | | $R_L = 2\text{ k}\Omega$ to GND $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | | | -4.75 | V |
| Short-Circuit Limit | I_{SC} | Source/sink | | ± 10 | | mA |
| Closed-Loop Impedance | Z_{OUT} | $f = 100\text{ kHz}$, $A_V = 1$ | | 71 | | Ω |
| POWER SUPPLY | | | | | | |
| Power Supply Rejection Ratio | PSRR | $V_{SY} = 3\text{ V to }36\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | 100 | | | dB |
| | | | 90 | | | dB |
| Supply Current per Amplifier | I_{SY} | $V_O = V_{SY}/2$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | | 47 | 55 | μA |
| | | | | | 75 | μA |
| DYNAMIC PERFORMANCE | | | | | | |
| Slew Rate | SR | $R_L = 100\text{ k}\Omega$, $C_L = 30\text{ pF}$ | | 0.3 | | $\text{V}/\mu\text{s}$ |
| Gain Bandwidth Product | GBP | $V_{IN} = 5\text{ mV p-p}$, $R_L = 10\text{ k}\Omega$, $A_V = 100$ | | 595 | | kHz |
| Unity-Gain Crossover | UGC | $V_{IN} = 5\text{ mV p-p}$, $R_L = 10\text{ k}\Omega$, $A_V = 1$ | | 550 | | kHz |
| Phase Margin | Φ_M | | | 52 | | Degrees |
| -3 dB Closed-Loop Bandwidth | $f_{-3\text{ dB}}$ | $A_V = 1$, $V_{IN} = 5\text{ mV p-p}$ | | 1140 | | kHz |
| NOISE PERFORMANCE | | | | | | |
| Voltage Noise | e_n p-p | 0.1 Hz to 10 Hz | | 0.7 | | $\mu\text{V p-p}$ |
| Voltage Noise Density | e_n | $f = 1\text{ kHz}$ | | 27 | | $\text{nV}/\sqrt{\text{Hz}}$ |
| Current Noise Density | i_n | $f = 1\text{ kHz}$ | | 0.2 | | $\text{pA}/\sqrt{\text{Hz}}$ |

ELECTRICAL SPECIFICATIONS, $V_{SY} = \pm 15\text{ V}$ $V_{SY} = \pm 15\text{ V}$, $V_{CM} = V_{SY}/2$, $V_O = 0.0\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.**Table 4.**

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---------------------------------|--------------------------|---|-------|-----------|-----------|------------------------------|
| INPUT CHARACTERISTICS | | | | | | |
| Offset Voltage | V_{OS} | $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | | 35 | 300 | μV |
| Offset Voltage Drift | $\Delta V_{OS}/\Delta T$ | | | 1 | 500 | $\mu\text{V}/^\circ\text{C}$ |
| Input Bias Current | I_B | $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | | ± 3 | ± 25 | nA |
| Input Offset Current | I_{OS} | $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | | ± 0.1 | ± 1.5 | nA |
| Input Voltage Range | | | -15 | | +15 | V |
| Common-Mode Rejection Ratio | CMRR | $V_{CM} = -15\text{ V to }+15\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | 81 | 95 | | dB |
| | | $V_{CM} = -13\text{ V to }+13\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | 75 | 107 | | dB |
| Large Signal Voltage Gain | A_{VO} | $R_L = 10\text{ k}\Omega$, $V_O = \pm 14.7\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | 89 | 120 | | dB |
| | | $R_L = 2\text{ k}\Omega$, $V_O = \pm 11\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | 109 | 112 | | dB |
| | | | 105 | | | dB |
| | | | 99 | | | dB |
| | | | 90 | | | dB |
| Input Capacitance | | | | | | |
| Differential Mode | C_{DM} | | | 2.5 | | pF |
| Common Mode | C_{CM} | | | 7 | | pF |
| MATCHING CHARACTERISTICS | | | | | | |
| Offset Voltage | | $T_A = 25^\circ\text{C}$ | | 100 | 300 | μV |
| OUTPUT CHARACTERISTICS | | | | | | |
| Output Voltage High | V_{OH} | $R_L = 10\text{ k}\Omega$ to GND $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | 14.92 | 14.94 | | V |
| | | $R_L = 2\text{ k}\Omega$ to GND $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | 14.90 | 14.3 | | V |
| | | | 14.0 | | | V |
| | | | 11.0 | | | V |
| Output Voltage Low | V_{OL} | $R_L = 10\text{ k}\Omega$ to GND $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | | -14.96 | -14.80 | V |
| | | $R_L = 2\text{ k}\Omega$ to GND $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | | -14.75 | -14.75 | V |
| | | | | -14.75 | -14.60 | V |
| | | | | | -14.0 | V |
| Short-Circuit Limit | I_{SC} | Source/sink | | ± 10 | | mA |
| Closed-Loop Impedance | Z_{OUT} | $f = 100\text{ kHz}$, $A_V = 1$ | | 40 | | Ω |
| POWER SUPPLY | | | | | | |
| Power Supply Rejection Ratio | PSRR | $V_{SY} = 3\text{ V to }36\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | 100 | | | dB |
| | | | 90 | | | dB |
| Supply Current per Amplifier | I_{SY} | $V_O = V_{SY}/2$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | | 60 | 75 | μA |
| | | | | | 100 | μA |
| DYNAMIC PERFORMANCE | | | | | | |
| Slew Rate | SR | $R_L = 100\text{ k}\Omega$, $C_L = 30\text{ pF}$ | | 0.4 | | V/ μ |
| Settling Time | t_S | To 0.1%, 10 V step | | 23.4 | | μs |
| Gain Bandwidth Product | GBP | $V_{IN} = 5\text{ mV p-p}$, $R_L = 10\text{ k}\Omega$, $A_V = 100$ | | 786 | | kHz |
| Unity-Gain Crossover | UGC | $V_{IN} = 5\text{ mV p-p}$, $R_L = 10\text{ k}\Omega$, $A_V = 1$ | | 800 | | kHz |
| Phase Margin | Φ_M | | | 60 | | Degrees |
| -3 dB Closed-Loop Bandwidth | $f_{-3\text{ dB}}$ | $A_V = 1$, $V_{IN} = 5\text{ mV p-p}$ | | 1520 | | kHz |
| Channel Separation | CS | $f = 1\text{ kHz}$ | | 100 | | dB |
| NOISE PERFORMANCE | | | | | | |
| Voltage Noise | e_n p-p | 0.1 Hz to 10 Hz | | 0.7 | | $\mu\text{V p-p}$ |
| Voltage Noise Density | e_n | $f = 1\text{ kHz}$ | | 27 | | nV/ $\sqrt{\text{Hz}}$ |
| Current Noise Density | i_n | $f = 1\text{ kHz}$ | | 0.2 | | pA/ $\sqrt{\text{Hz}}$ |

ABSOLUTE MAXIMUM RATINGS

Table 5.

| Parameter | Rating |
|--|---|
| Supply Voltage | 36 V |
| Input Voltage | |
| Operating Condition | $-V \leq V_{IN} \leq +V$ |
| Overvoltage Condition ¹ | $(-V) - 32 V \leq V_{IN} \leq (+V) + 32 V$ |
| Differential Input Voltage ² | $\pm V_{SY}$ |
| Input Current | $\pm 5 \text{ mA}$ |
| Output Short-Circuit Duration to GND | Indefinite |
| Storage Temperature Range | -65°C to $+150^{\circ}\text{C}$ |
| Operating Temperature Range | -40°C to $+125^{\circ}\text{C}$ |
| Junction Temperature Range | -65°C to $+150^{\circ}\text{C}$ |
| Lead Temperature (Soldering, 60 seconds) | 300°C |

¹ Performance not guaranteed during overvoltage conditions.

² Limit the input current to $\pm 5 \text{ mA}$.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the device soldered on a 4-layer JEDEC standard printed circuit board (PCB) with zero airflow. The exposed pad is soldered to the application board.

Table 6. Thermal Resistance

| Package Type | θ_{JA} | θ_{JC} | Unit |
|--------------------------|---------------|---------------|-----------------------------|
| 8-Lead MSOP (RM-8) | 142 | 45 | $^{\circ}\text{C}/\text{W}$ |
| 8-Lead LFCSP (CP-8-10) | 76 | 43 | $^{\circ}\text{C}/\text{W}$ |
| 14-Lead TSSOP (RU-14) | 112 | 35 | $^{\circ}\text{C}/\text{W}$ |
| 16-Lead LFCSP (CP-16-27) | 75 | 12 | $^{\circ}\text{C}/\text{W}$ |

ESD CAUTION

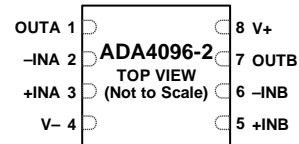


ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



Figure 4. 8-Lead, MSOP (RM-8), ADA4096-2



NOTES
1. CONNECT THE EXPOSED PAD TO V-.

Figure 5. 8-Lead LFCSP (CP-8-10), ADA4096-2

Table 7. Pin Function Descriptions, ADA4096-2

| Pin No. ¹ | | Mnemonic | Description |
|----------------------|-----------------|----------|---|
| 8-Lead MSOP | 8-Lead LFCSP | | |
| 1 | 1 | OUTA | Output Channel A. |
| 2 | 2 | -INA | Negative Input Channel A. |
| 3 | 3 | +INA | Positive Input Channel A. |
| 4 | 4 | V- | Negative Supply Voltage. |
| 5 | 5 | +INB | Positive Input Channel B. |
| 6 | 6 | -INB | Negative Input Channel B. |
| 7 | 7 | OUTB | Output Channel B. |
| 8 | 8 | V+ | Positive Supply Voltage. |
| N/A | EP ² | EPAD | Exposed Pad. ² For the ADA4096-2 (8-lead LFCSP only), connect the exposed pad to V-. |

¹ N/A means not applicable.

² The exposed pad is not shown in the pin configuration diagram.

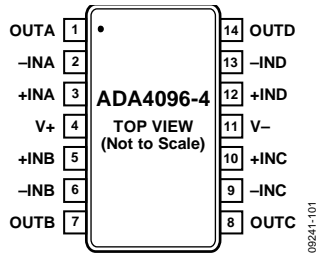
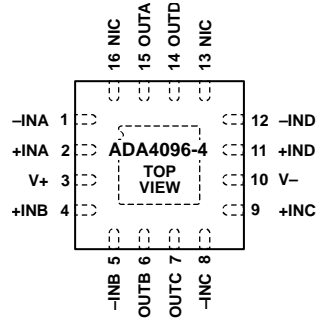


Figure 6. 14-Lead TSSOP (RU-14), ADA4096-4



NOTES
 1. NIC = NOT INTERNALLY CONNECTED.
 2. CONNECT THE EXPOSED PAD TO V-.

Figure 7. 16-Lead LFCSP (CP-16-27), ADA4096-4

Table 8. Pin Function Descriptions, ADA4096-4

| Pin No. ¹ | | Mnemonic | Description |
|----------------------|-----------------|----------|--|
| 14-Lead TSSOP | 16-Lead LFCSP | | |
| 1 | 15 | OUTA | Output Channel A. |
| 2 | 1 | -INA | Negative Input Channel A. |
| 3 | 2 | +INA | Positive Input Channel A. |
| 4 | 3 | V+ | Positive Supply Voltage. |
| 5 | 4 | +INB | Positive Input Channel B. |
| 6 | 5 | -INB | Negative Input Channel B. |
| 7 | 6 | OUTB | Output Channel B. |
| 8 | 7 | OUTC | Output Channel C. |
| 9 | 8 | -INC | Negative Input Channel C. |
| 10 | 9 | +INC | Positive Input Channel C. |
| 11 | 10 | V- | Negative Supply Voltage. |
| 12 | 11 | +IND | Positive Input Channel D. |
| 13 | 12 | -IND | Negative Input Channel D. |
| 14 | 14 | OUTD | Output Channel D. |
| N/A | 13 | NIC | No Internal Connection. |
| N/A | 16 | NIC | No Internal Connection. |
| N/A | EP ² | EPAD | Exposed Pad. ² For the ADA4096-4 (16-lead LFCSP only), connect the exposed pad to V-. |

¹ N/A means not applicable.

² The exposed pad is not shown in the pin configuration diagram.

TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25^\circ\text{C}$, unless otherwise noted. All typical performance characteristics shown are for the ADA4096-2 only.

$\pm 1.5\text{ V}$ CHARACTERISTICS

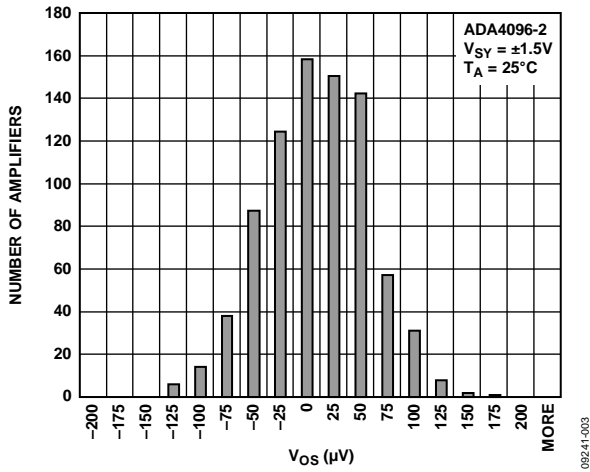


Figure 8. Input Offset Voltage (V_{OS}) Distribution

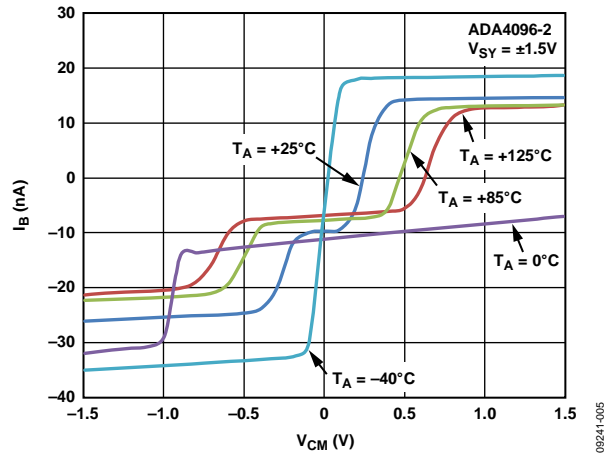


Figure 11. Input Bias Current (I_B) vs. V_{CM} for Various Temperatures

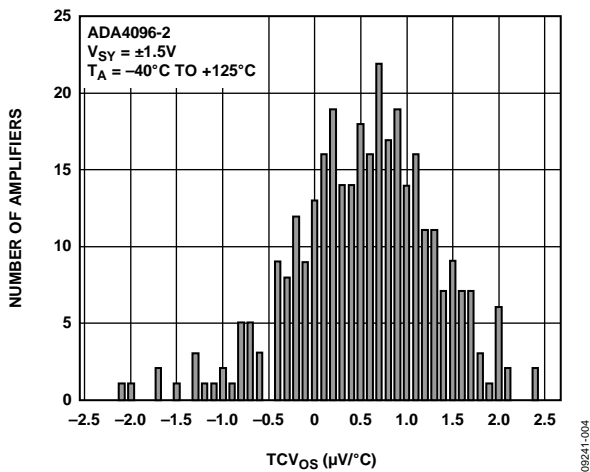


Figure 9. Offset Voltage Drift (TCV_{OS}) Distribution

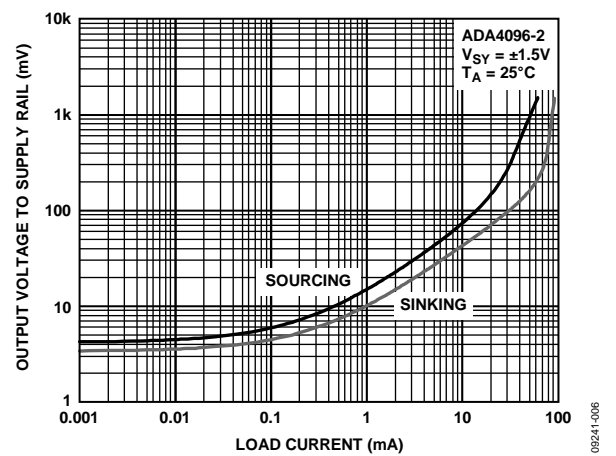


Figure 12. Output Voltage to Supply Rail vs. Load Current

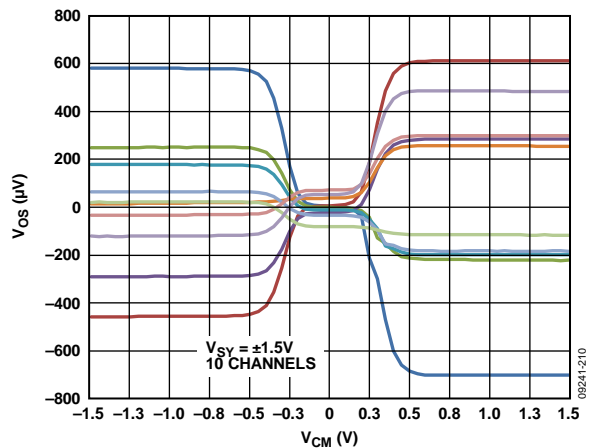


Figure 10. Input Offset Voltage (V_{OS}) vs. Common-Mode Voltage (V_{CM})

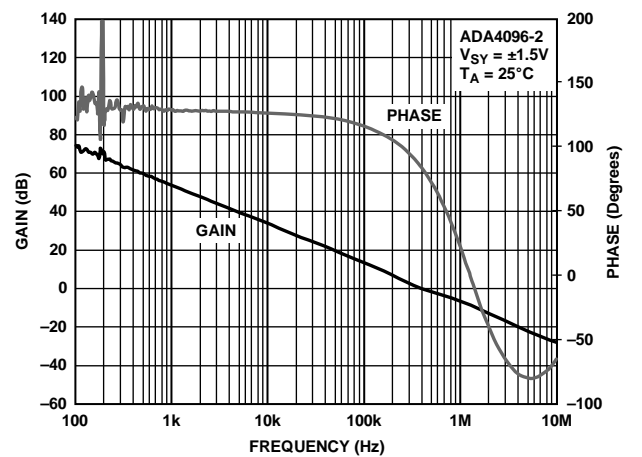


Figure 13. Open-Loop Gain and Phase vs. Frequency

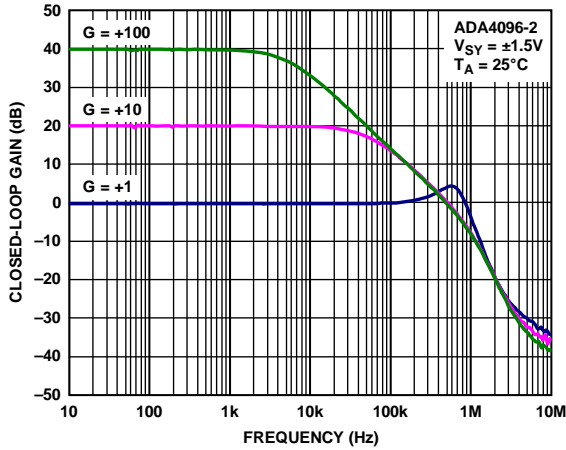


Figure 14. Closed-Loop Gain vs. Frequency

09241-008

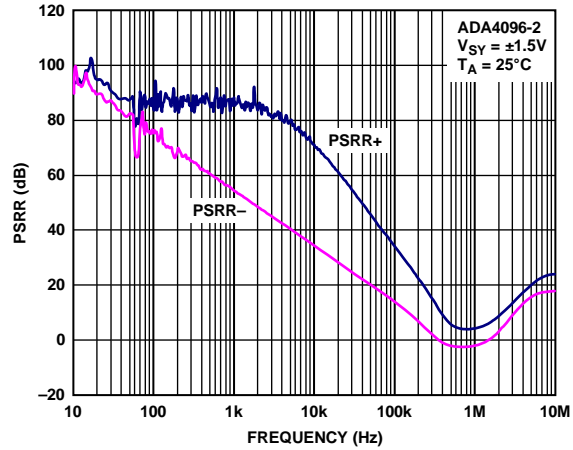


Figure 16. PSRR vs. Frequency

09241-052

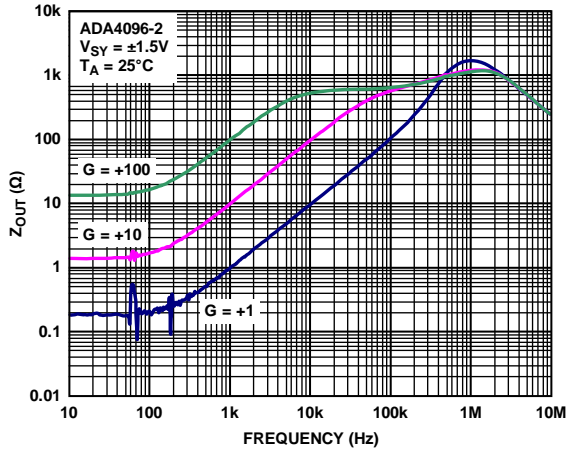


Figure 15. Output Impedance (Z_{out}) vs. Frequency

09241-009

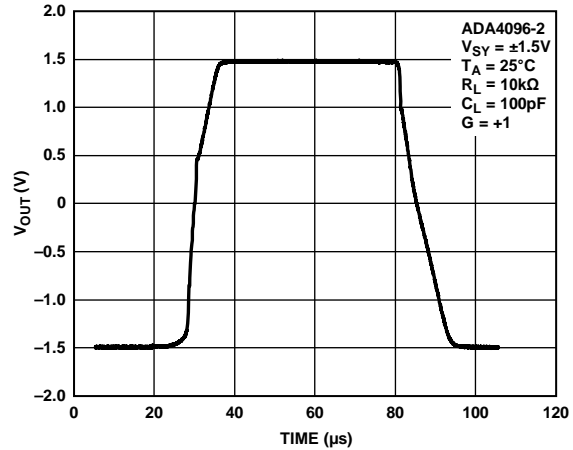


Figure 17. Large Signal Transient Response

09241-010

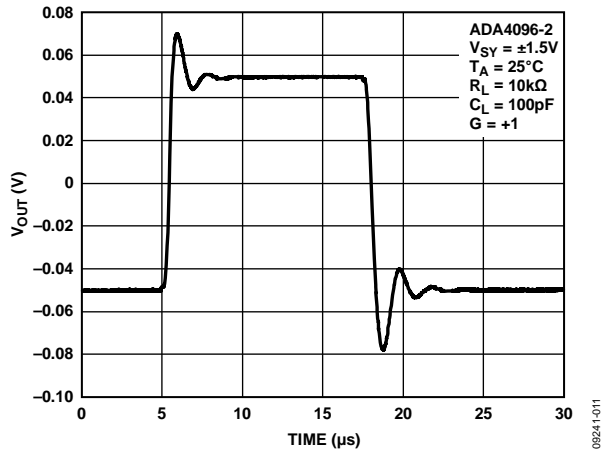


Figure 18. Small Signal Transient Response

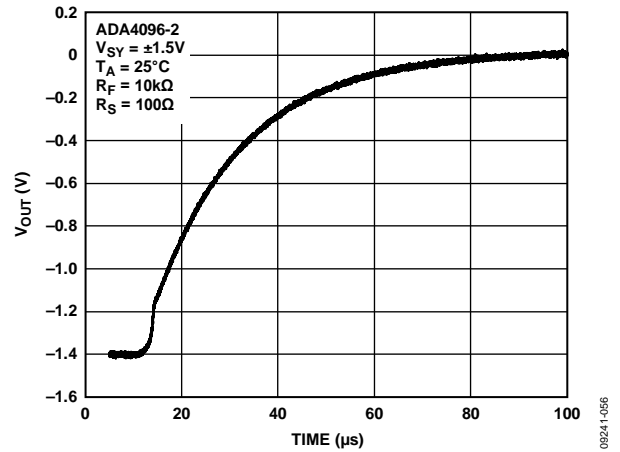


Figure 20. Negative Overload Recovery

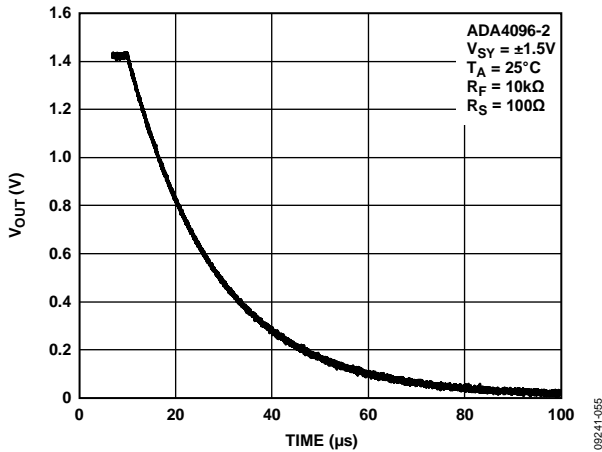


Figure 19. Positive Overload Recovery

±5 V CHARACTERISTICS

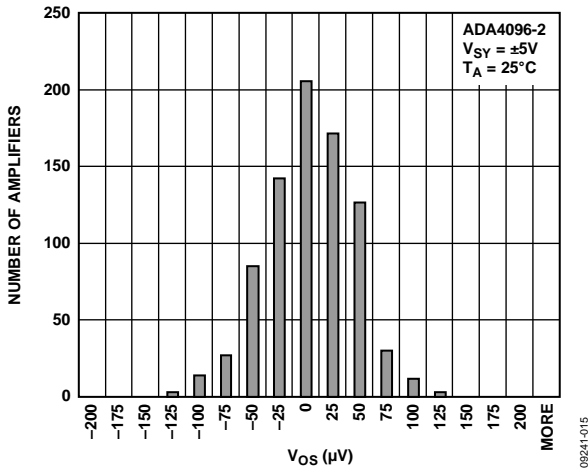


Figure 21. Input Offset Voltage (V_{OS}) Distribution

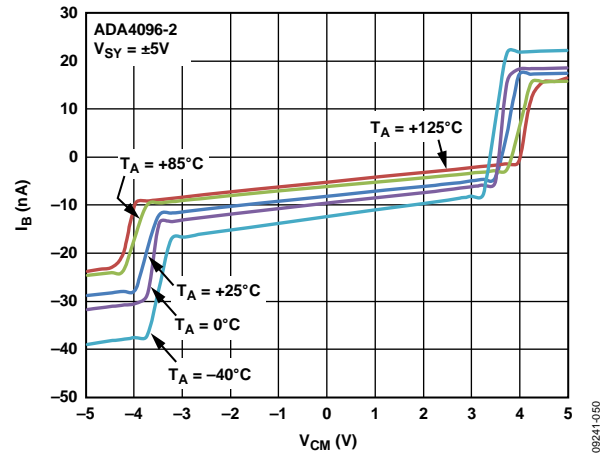


Figure 24. Input Bias Current (I_B) vs. V_{CM} for Various Temperatures

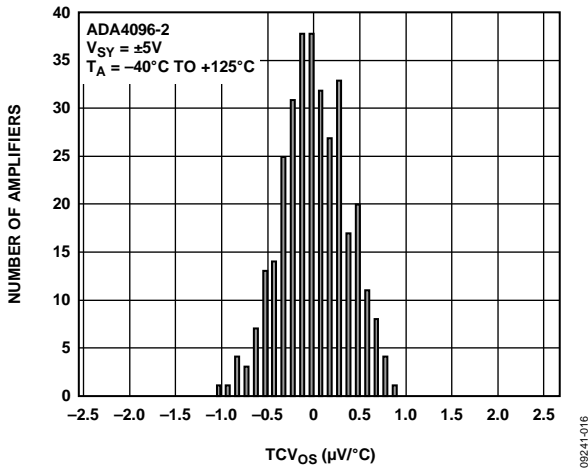


Figure 22. Offset Voltage Drift (TCV_{OS}) Distribution

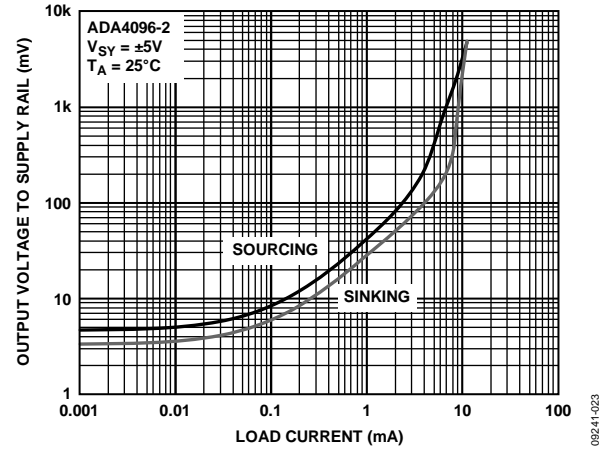


Figure 25. Output Voltage to Supply Rail vs. Load Current

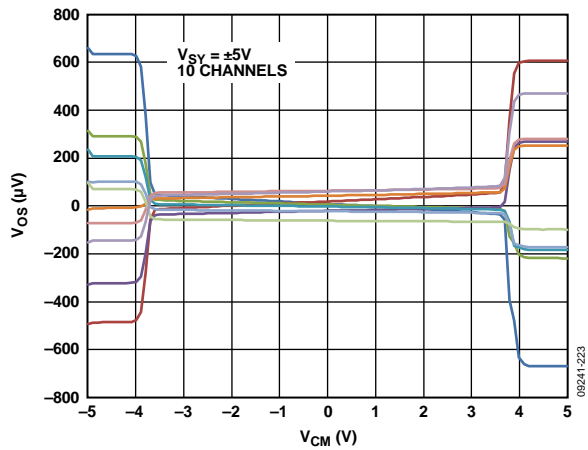


Figure 23. Input Offset Voltage (V_{OS}) vs. Common-Mode Voltage (V_{CM})

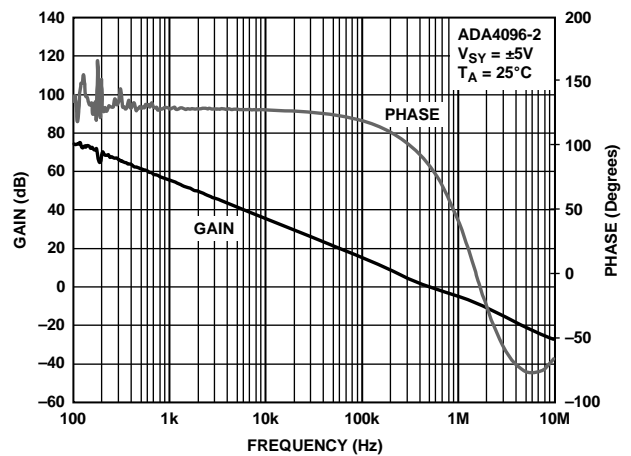


Figure 26. Open-Loop Gain and Phase vs. Frequency.

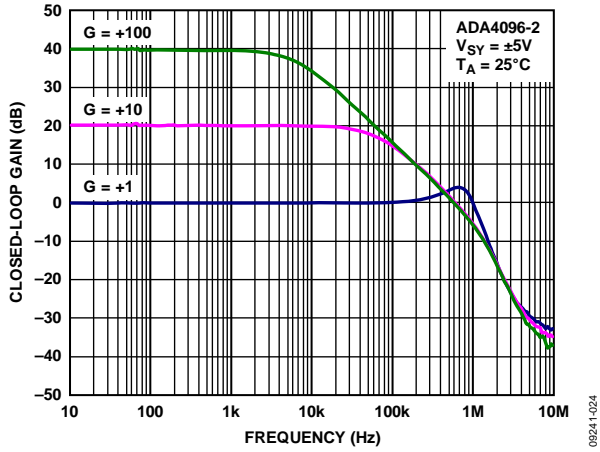


Figure 27. Closed-Loop Gain vs. Frequency

09241-024

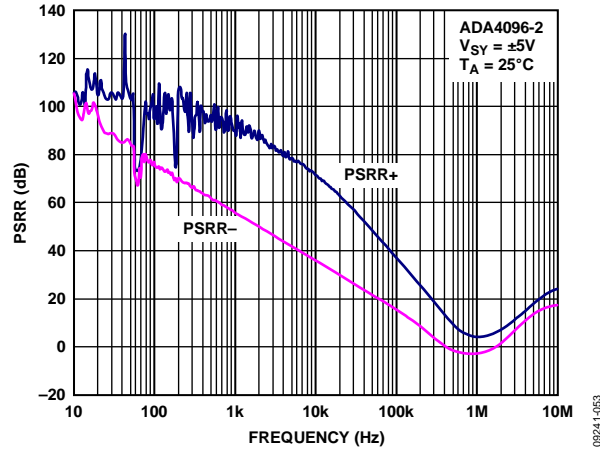


Figure 29. PSRR vs. Frequency

09241-053

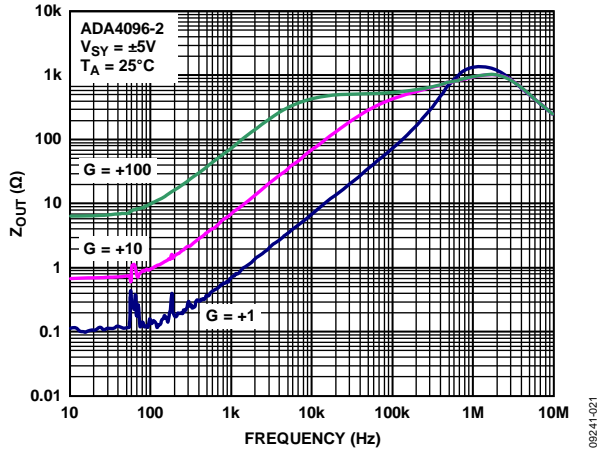


Figure 28. Output Impedance (Z_{out}) vs. Frequency.

09241-021

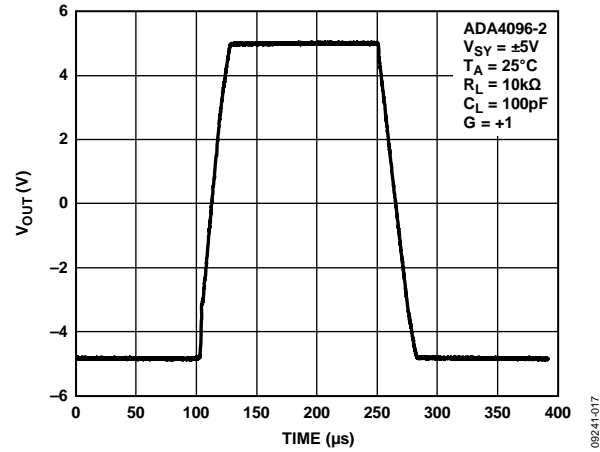


Figure 30. Large Signal Transient Response

09241-017

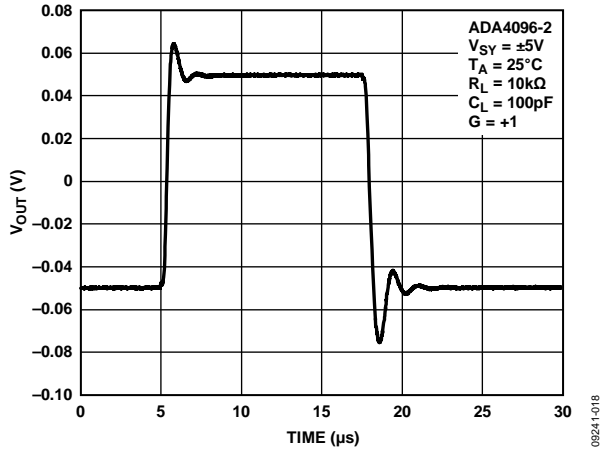


Figure 31. Small Signal Transient Response

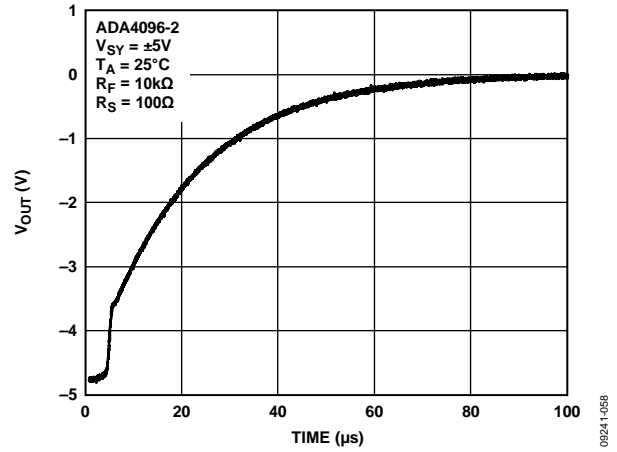


Figure 33. Negative Overload Recovery

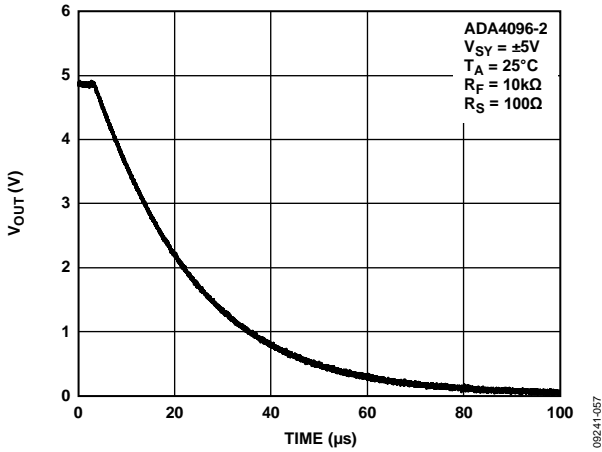


Figure 32. Positive Overload Recovery

09241-018

09241-058

09241-057

±15 V CHARACTERISTICS

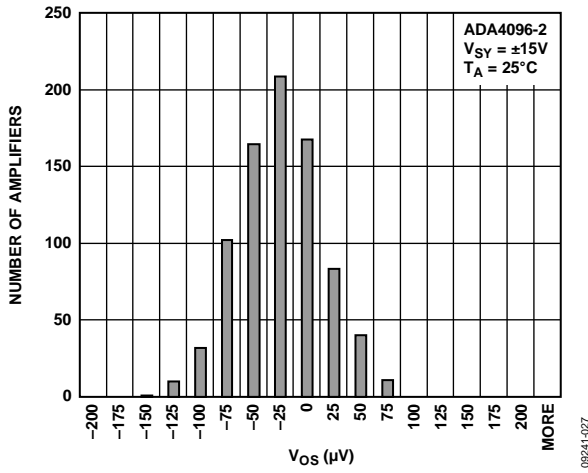


Figure 34. Input Offset Voltage (V_{OS}) Distribution

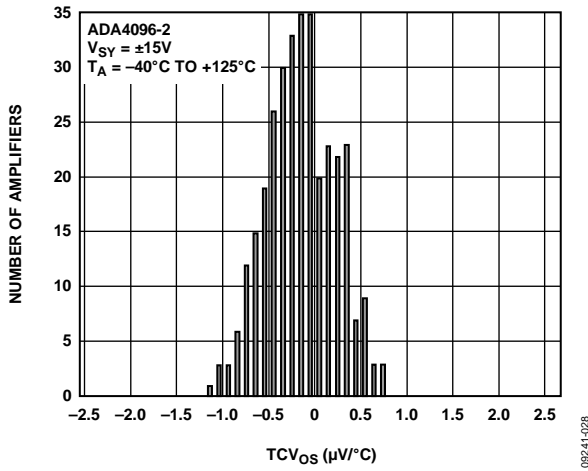


Figure 35. Offset Voltage Drift (TCV_{OS}) Distribution

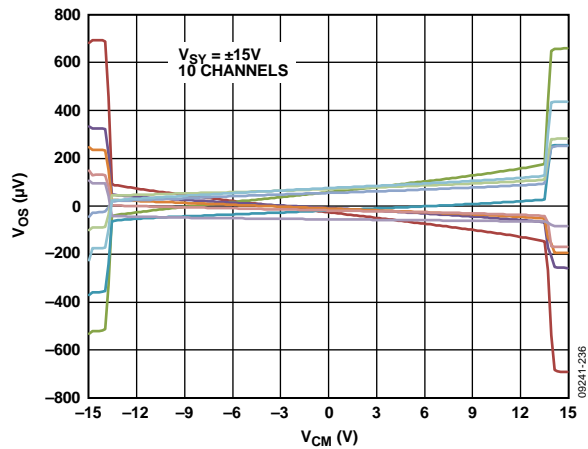


Figure 36. Input Offset Voltage (V_{OS}) vs. Common-Mode Voltage (V_{CM})

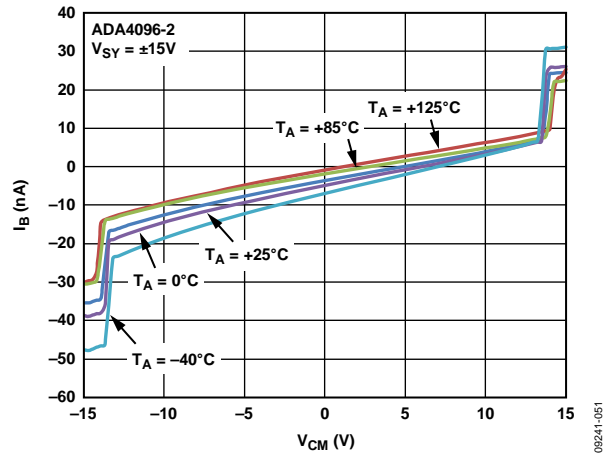


Figure 37. Input Bias Current (I_B) vs. V_{CM} for Various Temperatures

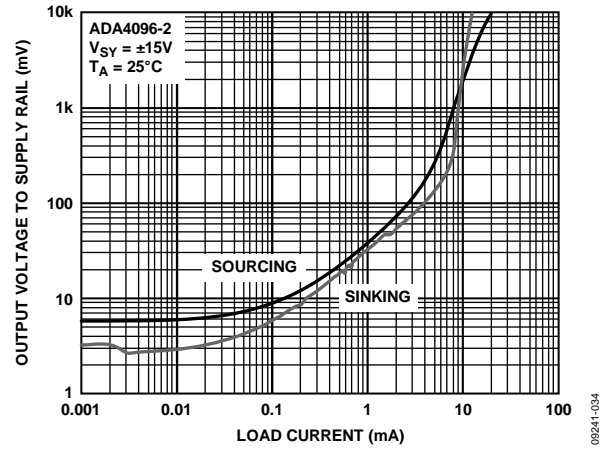


Figure 38. Output Voltage to Supply Rail vs. Load Current

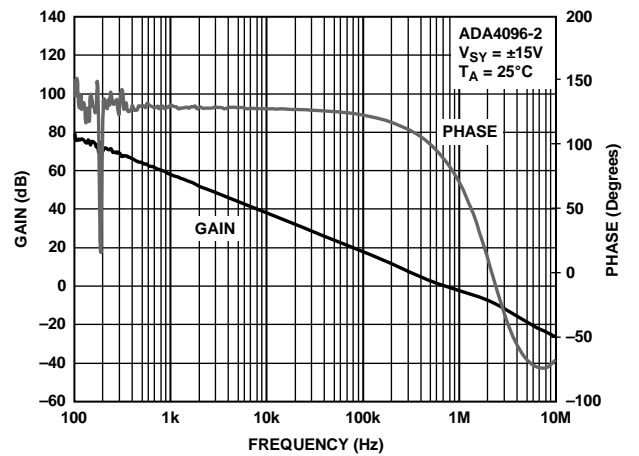


Figure 39. Open-Loop Gain and Phase vs. Frequency

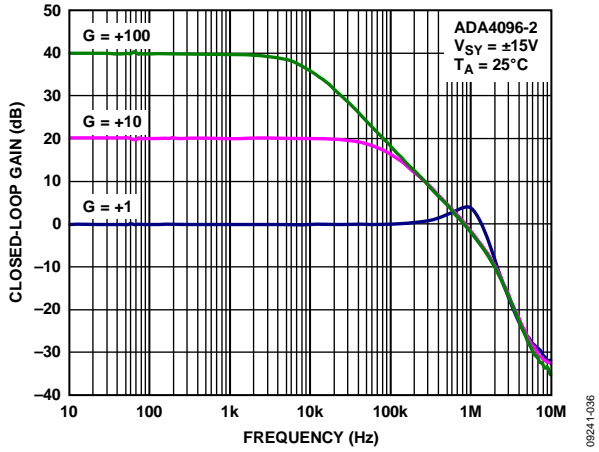


Figure 40. Closed-Loop Gain vs. Frequency

09241-036

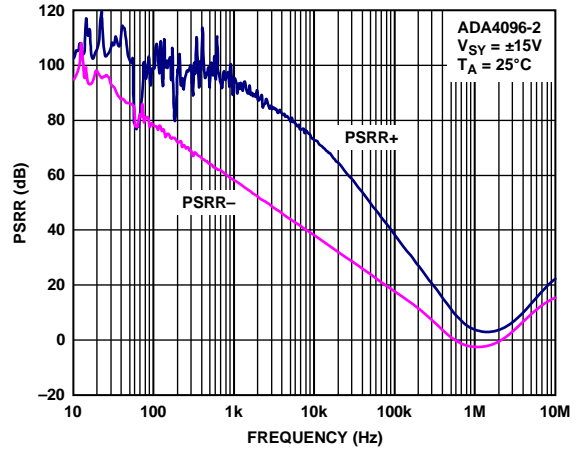


Figure 42. PSRR vs. Frequency

09241-054

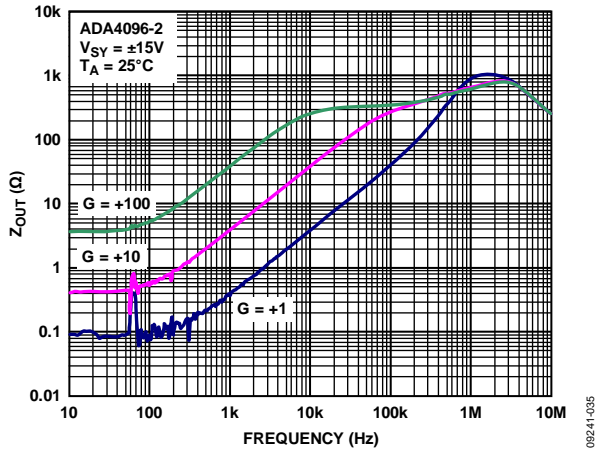


Figure 41. Output Impedance (Z_{OUT}) vs. Frequency

09241-035

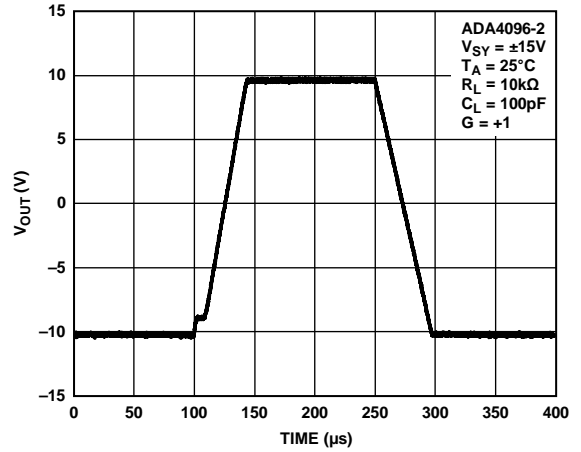


Figure 43. Large Signal Transient Response

09241-031

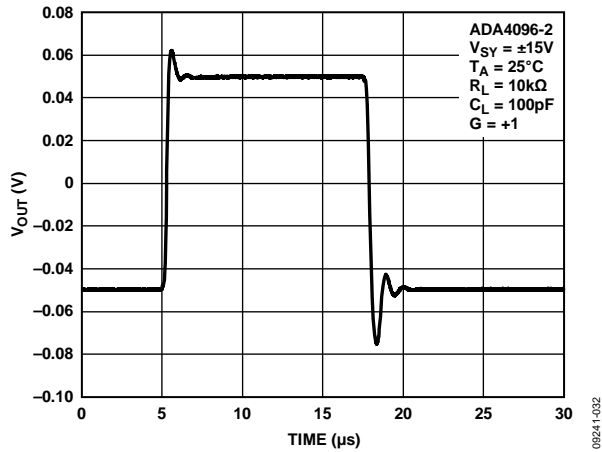


Figure 44. Small Signal Transient Response

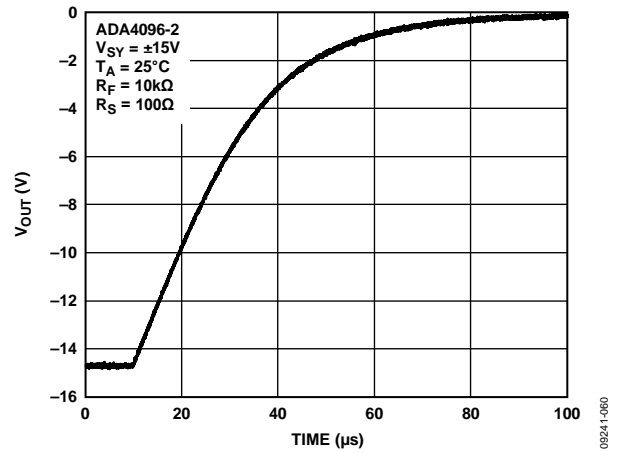


Figure 46. Negative Overload Recovery

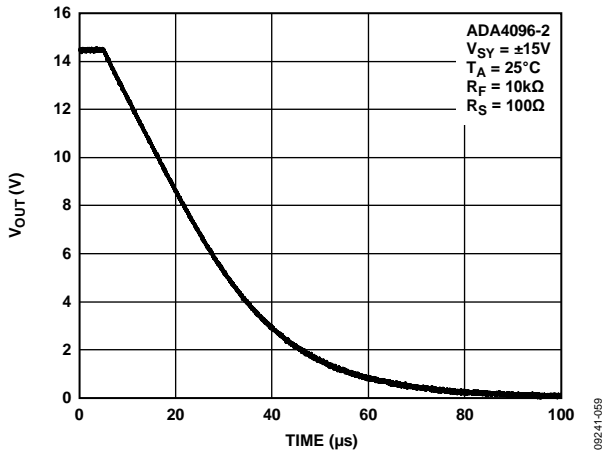


Figure 45. Positive Overload Recovery

COMPARATIVE VOLTAGE AND VARIABLE VOLTAGE GRAPHS

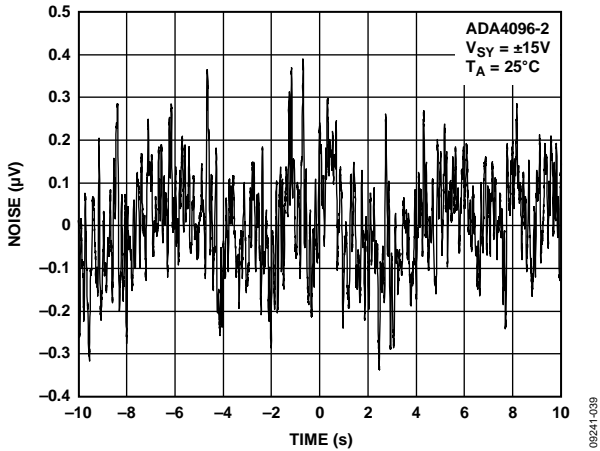


Figure 47. Input Voltage Noise, 0.1 Hz to 10 Hz Bandwidth

09241-039

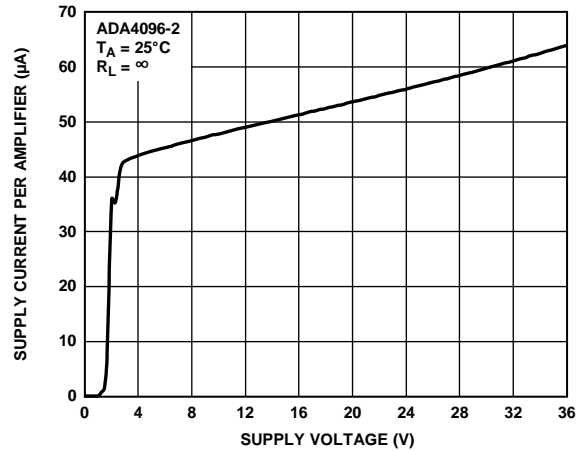


Figure 50. Supply Current per Amplifier vs. Supply Voltage

09241-043

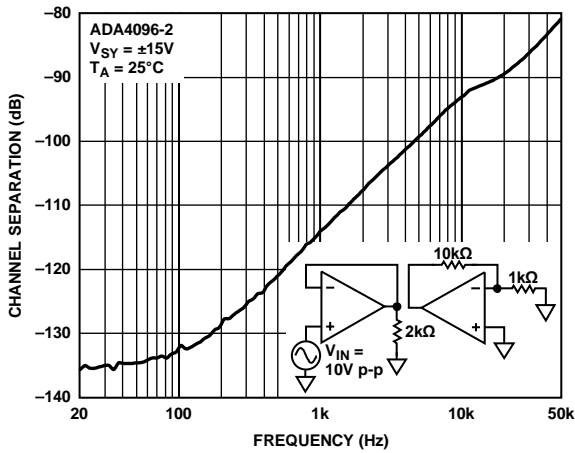


Figure 48. Channel Separation vs. Frequency

09241-040

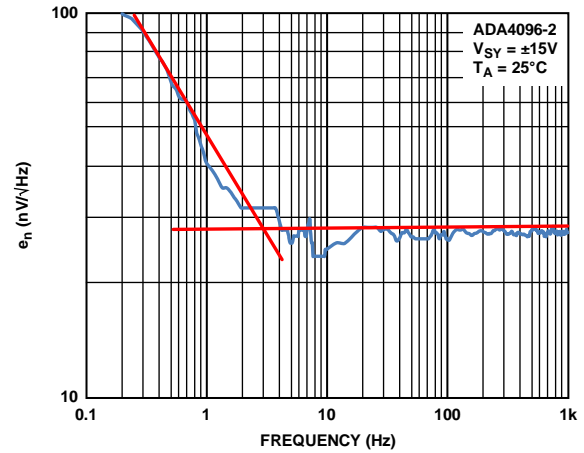


Figure 51. Voltage Noise Density (e_n) vs. Frequency

09241-044

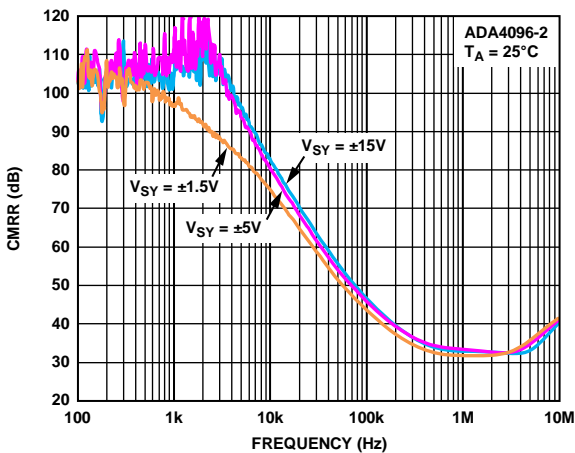


Figure 49. CMRR vs. Frequency

09241-041

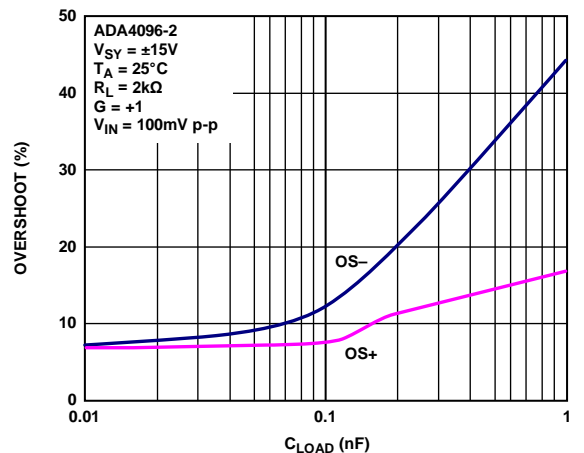


Figure 52. Overshoot vs. Load Capacitance (C_{LOAD})

09241-100

THEORY OF OPERATION

INPUT STAGE

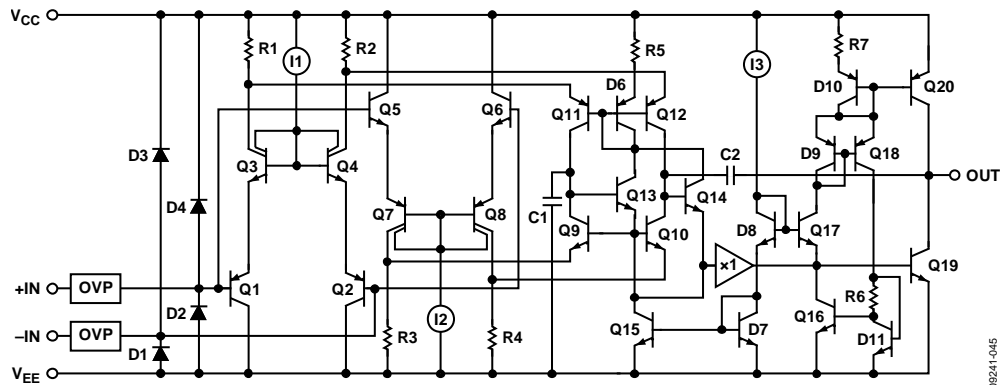


Figure 53. Simplified Schematic, ADA4096-2

Figure 53 shows a simplified schematic of the ADA4096-2. The input stage comprises two differential pairs (Q1 to Q4 and Q5 to Q8) operating in parallel. When the input common-mode voltage approaches $V_{CC} - 1.5\text{ V}$, Q1 to Q4 shut down as I1 reaches its minimum voltage compliance. Conversely, when the input common-mode voltage approaches $V_{EE} + 1.5\text{ V}$, Q5 to Q8 shut down as I2 reaches its minimum voltage compliance. This topology allows for maximum input dynamic range because the amplifier can function with its inputs at 200 mV outside the rail (at room temperature).

As with any rail-to-rail input amplifier, V_{OS} mismatch between the two input pairs determines the CMRR of the amplifier. If the input common-mode voltage range is kept within 1.5 V of each rail, transitions between the input pairs are avoided, thus improving the CMRR by approximately 10 dB (see Table 3 and Table 4).

PHASE INVERSION

Some single-supply amplifiers exhibit phase inversion when the input signal extends beyond the common-mode voltage range of the amplifier. When the input devices become saturated, the inverting and noninverting inputs exchange functions, causing the output to move in the opposing direction.

Although phase inversion persists for only as long as the inputs are saturated, it can be detrimental to applications where the amplifier is part of a closed-loop system. The ADA409x family is free from phase inversion over the entire common-mode voltage range, as well as the overvoltage protected range that is stated in the Absolute Maximum Ratings section, Table 5. Figure 54 shows the ADA4096-2 in a unity-gain configuration with the input signal at $\pm 40\text{ V}$ and the amplifier supplies at $\pm 10\text{ V}$.

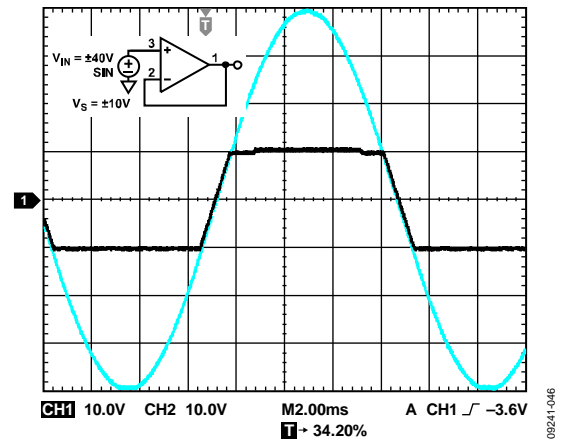


Figure 54. No Phase Reversal

INPUT OVERVOLTAGE PROTECTION

The ADA409x family inputs are protected from input voltage excursions up to 32 V outside each rail. This feature is of particular importance in applications with power supply sequencing issues that could cause the signal source to be active before the power supplies.

Figure 55 shows the input current limiting capability of the ADA4096-2 (green curves) compared to using a 5 kΩ series resistor (red curves).

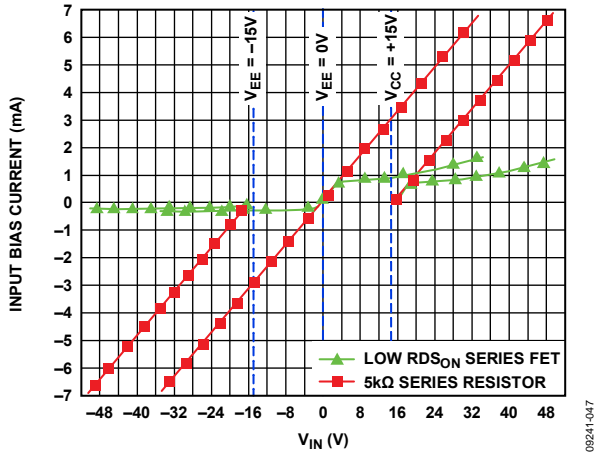


Figure 55. Input Current Limiting Capability

Figure 55 was generated with the ADA4096-2 in a buffer configuration with the supplies connected to GND (or ±15 V) and the positive input swept until it exceeds the supplies by 32 V. In general, input current is limited to 1 mA during positive overvoltage conditions and 200 μA during negative undervoltage conditions. For example, at an overvoltage of 20 V, the ADA4096-2 input current is limited to 1 mA, providing a current-limit equivalent to a series 20 kΩ resistor. Figure 55 also shows that the current limiting circuitry is active whether the amplifier is powered or not.

Note that Figure 55 represents input protection under abnormal conditions only. The correct amplifier operation input voltage range (IVR) is specified in Table 2 to Table 4.

COMPARATOR OPERATION

Although op amps are quite different from comparators, occasionally an unused section of a dual or a quad op amp may be pressed into service as a comparator; however, this is not recommended for any rail-to-rail output op amps. For rail-to-rail output op amps, the output stage is generally a ratioed current mirror with bipolar or metal-oxide semiconductor field-effect transistor (MOSFET) transistors. With the device operating in open loop, the second stage increases the current drive to the ratioed mirror to close the loop, but it cannot, which results in an increase in supply current. With the op amp configured as a comparator, the supply current can be significantly higher (see Figure 56).

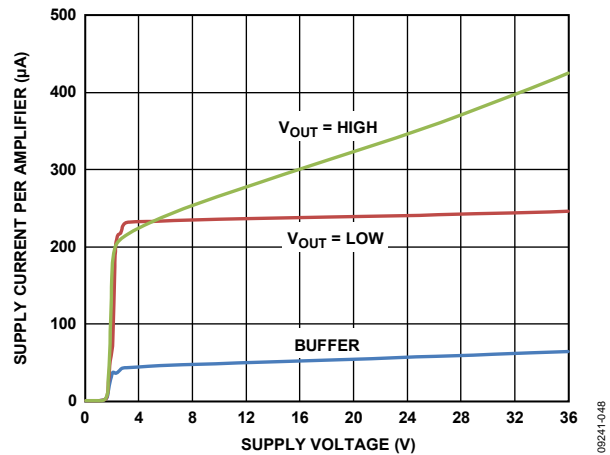
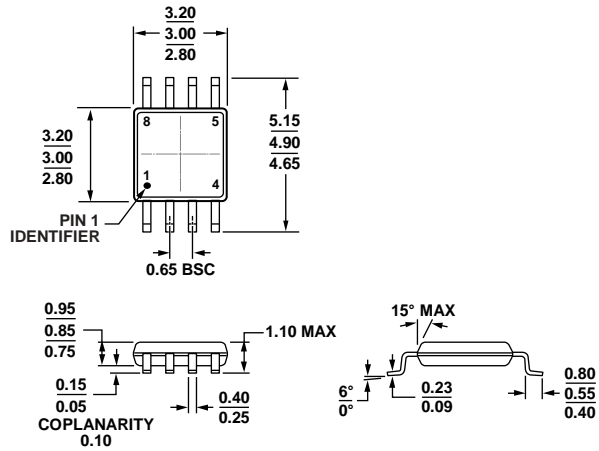


Figure 56. Comparator Supply Current

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 57. 8-Lead Mini Small Outline Package [MSOP] (RM-8)

Dimensions shown in millimeters

10-07-2009-B

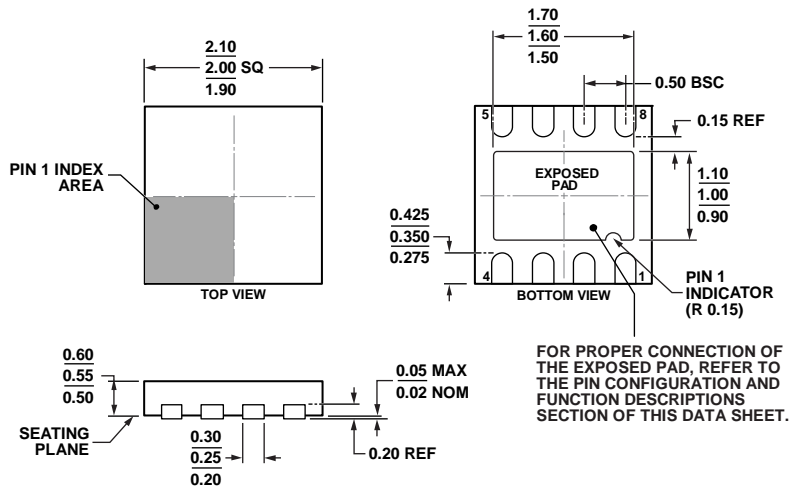
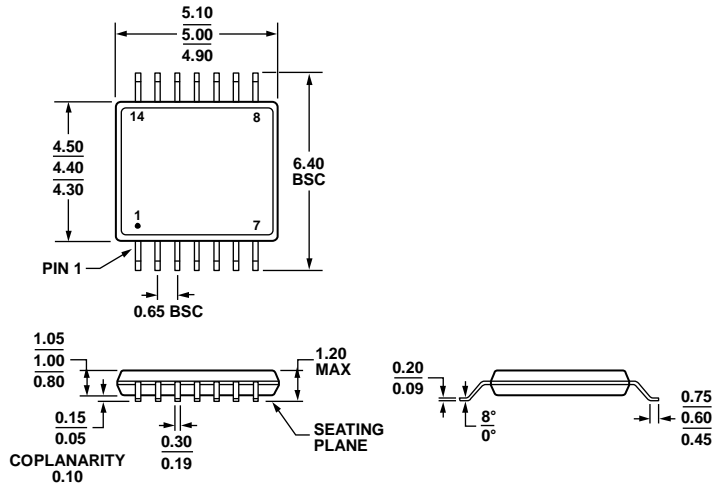


Figure 58. 8-Lead Lead Frame Chip Scale Package [LFCSP_UD] 2 mm x 2 mm Body, Ultra Thin, Dual Lead (CP-8-10)

Dimensions shown in millimeters

01-14-2013-C

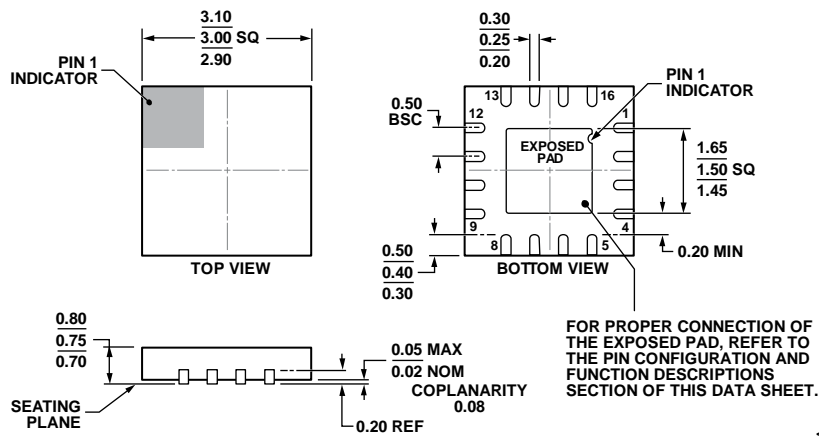


COMPLIANT TO JEDEC STANDARDS MO-153-AB-1

Figure 59. 14-Lead Thin Shrink Small Outline Package [TSSOP] (RU-14)

Dimensions shown in millimeters

061908-A



COMPLIANT TO JEDEC STANDARDS MO-220-WEED-6.

Figure 60. 16-Lead Lead Frame Chip Scale Package [LF CSP_WQ] 3 mm x 3 mm Body, Very Very Thin Quad (CP-16-27)

Dimensions shown in millimeters

01-26-2012-A

ORDERING GUIDE

| Model ^{1,2} | Temperature Range | Package Description | Package Option | Branding |
|----------------------|-------------------|---|----------------|----------|
| ADA4096-2ARMZ | -40°C to +125°C | 8-Lead Mini Small Outline Package [MSOP] | RM-8 | A2T |
| ADA4096-2ARMZ-R7 | -40°C to +125°C | 8-Lead Mini Small Outline Package [MSOP] | RM-8 | A2T |
| ADA4096-2ARMZ-RL | -40°C to +125°C | 8-Lead Mini Small Outline Package [MSOP] | RM-8 | A2T |
| ADA4096-2ACPZ-R7 | -40°C to +125°C | 8-Lead Lead Frame Chip Scale Package [LFCSP_UD] | CP-8-10 | A4 |
| ADA4096-2ACPZ-RL | -40°C to +125°C | 8-Lead Lead Frame Chip Scale Package [LFCSP_UD] | CP-8-10 | A4 |
| ADA4096-2WARMZ-R7 | -40°C to +125°C | 8-Lead Mini Small Outline Package [MSOP] | RM-8 | A2T |
| ADA4096-2WARMZ-RL | -40°C to +125°C | 8-Lead Mini Small Outline Package [MSOP] | RM-8 | A2T |
| ADA4096-4ARUZ | -40°C to +125°C | 14-Lead Thin Shrink Small Outline Package [TSSOP] | RU-14 | |
| ADA4096-4ARUZ-R7 | -40°C to +125°C | 14-Lead Thin Shrink Small Outline Package [TSSOP] | RU-14 | |
| ADA4096-4ARUZ-RL | -40°C to +125°C | 14-Lead Thin Shrink Small Outline Package [TSSOP] | RU-14 | |
| ADA4096-4ACPZ-R7 | -40°C to +125°C | 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ] | CP-16-27 | A30 |
| ADA4096-4ACPZ-RL | -40°C to +125°C | 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ] | CP-16-27 | A30 |

¹ Z = RoHS Compliant Part.

² W = Qualified for Automotive Applications.

AUTOMOTIVE PRODUCTS

The [ADA4096-2W](#) models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

NOTES